

CIRCUIT AND METHOD FOR AN INTEGRATED CHARGED DEVICE MODEL CLAMP

TECHNICAL FIELD

5 The present invention relates generally to integrated circuits, and more particularly to a circuit and method for an integrated charged device model clamp.

BACKGROUND

10 Integrated circuit ("IC") technology continues to improve, resulting in ICs with increasing density and devices with smaller and smaller geometries. As the devices become more miniaturized, however, they generally become more susceptible to electrostatic discharge ("ESD") damage. If ESD is not properly contained, it can lower a device's reliability or even destroy the device.

15 An ESD event typically occurs when an IC (e.g., a metal oxide semiconductor ("MOS") IC) is handled by a human being or by a machine. During an ESD event, a large voltage is applied to the IC. Generally, to avoid damage to the IC during an ESD event, ESD protection devices are typically fabricated on the IC and connected to the IC input/output pads and input/output circuits and other internal nodes of the IC. As used
20 herein with respect to a component in an IC, the phrase "input/output" means that the component is used for either input or output, or both. ESD protection devices generally provide discharge paths so that the internal circuits of the IC are not damaged during the ESD event.

25 Different ESD tests may be used to evaluate the effectiveness of ESD protection devices. Three ESD tests typically used include: the human body model ("HBM") test, a machine model ("MM") test and a charged device model ("CDM") test. Different ESD protection devices may be needed to optimize the level of ESD protection provided for the different ESD tests.

30 A detailed description of CDM events and IC design guidelines is provided in Timothy Maloney, "Designing MOS Inputs and Outputs to Avoid Oxide Failure in the Charged Device Model," EOS/ESD SYMPOSIUM PROCEEDINGS, 1988, pp. 220-27.

Generally, a CDM test simulates a charged device contacting a grounded surface (e.g., metal), typically associated with automated handling equipment in the production/manufacturing environment. A CDM test may be performed in the following manner. First, the device to be tested is charged. Most of this charge is stored in the VDD voltage supply rail and/or the ground supply rail within the device. Then one of the pads of the charged device is connected to an external ground. The charges stored in the VDD and/or ground supply rail then find pathways flowing to the pad under test, typically dissipating the charge within nanoseconds, thus testing the ESD protection devices implemented in the IC.

While primary ESD structures (e.g., PDNMOS, BTNMOS, dual-diodes) placed near the input/output pads of a device generally provide protection against HBM and MM events, they do not necessarily provide sufficient protection against CDM events. Generally, the most common damage caused by a CDM event is the rupture of thin dielectrics in the IC, such as MOS gate dielectrics or capacitor dielectrics. CDM clamps are therefore used to provide protection of internal IC input circuits against charged device ESD events. Generally, in prior art circuits, the CDM clamp devices are separated from the internal input circuit transistors, with a metal interconnect system providing the connections between the CDM clamps and the input circuit.

A disadvantage of the prior art circuits is that the metal/contact/via physical characteristics of this metal interconnect system may significantly increase the parasitic resistance and inductance of the circuit. Generally, in order for CDM clamps to be effective, the parasitic resistance and inductance between the ground/power-supply connections of the internal input circuit and the ground/power-supply connections of the CDM clamps must be minimized. Because the input circuitry may not reside in close physical proximity to its CDM ESD protection structure, however, there may be significant parasitic resistance and inductance in the metal ground bus between the CDM ESD structure and the input circuit inverter/buffer.

Generally, the parasitic inductance and resistance between the ground connection of the CDM clamp and the ground connection of the input circuit act in series with the clamp voltage of the CDM clamp, building up excess voltage across the pin being protected and ground. Likewise, the parasitic inductance and resistance between

- the power-supply connection of the CDM clamp and the power-supply connection of the input circuit act in series with the clamp voltage of the CDM clamp, building up excess voltage. Because a CDM event may have a peak current level of about 5-10 amps, with a rise time of a few hundred picoseconds, the voltage drop along the ground/power-supply bus metallization may be significant with respect to the CDM clamp voltage. The total voltage drop may be high enough to degrade or rupture the gate oxides of the input transistors.
- 5

Copyright © 2000 Texas Instruments Incorporated

SUMMARY OF THE INVENTION

These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present invention in which a CDM clamp circuit is integrated into the interface circuit being protected on the IC. Generally, the integrated CDM clamp circuit and interface circuit are adjacent to each other and share a common device element or component, thus eliminating the need for a metal interconnect. Because there is no interconnect, the parasitic resistance and inductance are also minimized or eliminated from the circuit, thus reducing or eliminating the excessive voltage drop present in prior art circuits.

Preferably, the CDM clamp circuit is integrated into the circuit that it is protecting by having the two circuits share the same silicon source region. In a preferred embodiment input circuit, the same diffusion region is the source of both the input transistor and its associated CDM clamp transistor. In one preferred embodiment, a PMOS input transistor and a PMOS CDM clamp transistor share a single p+ diffusion region. In another preferred embodiment, an NMOS input transistor and a NMOS CDM clamp transistor share a single n+ diffusion region.

An advantage of a preferred embodiment of the present invention is that it generally eliminates the need for a metal interconnect between the sources of the CDM clamp device and the internal circuit device.

Another advantage of a preferred embodiment of the present invention is that, by eliminating the source metal interconnect, it generally minimizes or eliminates parasitic resistance and inductance between the ground/power-supply connection of the internal input circuitry and the ground/power-supply connection of the CDM clamp device.

Another advantage of a preferred embodiment of the present invention is that it reduces the area on the IC needed for CDM protection because the devices are located directly adjacent to each other and because each CDM clamp shares a source region with the transistor that it is protecting.

The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be

described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also
5 be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

TI-31026 5

BRIEF DESCRIPTION OF THE DRAWING

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

FIGURE 1 is a schematic of an IC input circuit with CDM clamps;

FIGURE 2 is a schematic of a transistor implementation of a diode-to-ground CDM clamp;

FIGURE 3A is a cross-sectional view of a diode-to-supply CDM clamp;

FIGURE 3B is a schematic of a transistor implementation of a diode-to-supply CDM clamp;

FIGURE 4A is a schematic of an IC input circuit with MOS transistor CDM clamps;

FIGURE 4B is a plan view of an IC input circuit with integrated CDM clamps; and

FIGURE 4C is a cross-sectional view of an IC input circuit with integrated CDM clamps.

DETAILED DESCRIPTION

The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

The present invention will be described with respect to preferred embodiments in a specific context, namely an IC input circuit comprising PMOS and NMOS input transistors, with PMOS and NMOS CDM clamp transistors sharing the source diffusion regions of the respective input transistors. Preferred embodiments of the invention may be applied, however, to other integrated ESD and interface circuits. For example, the preferred embodiments may be applied to MOS, CMOS or BiCMOS ICs. Preferred embodiments may be applied to other field effect devices or to advanced bipolar technologies. In addition, preferred embodiments may be used to protect other IC interface circuits connected to the pads of the IC, such as input/output ("I/O") circuits or output circuits.

With reference now to Fig. 1, there is shown a schematic of a CDM protection scheme for an IC MOS input circuit. The input circuit comprises PMOS input transistor 102 and NMOS input transistor 104. Output 108 is connected to other internal IC circuitry. CDM clamp diodes 114 and 116 are connected to input transistors 102 and 104, respectively, to provide protection against CDM events. Input 106 is connected to IC input pad 110 via input resistor 112. Input resistor 112 is chosen so as to limit the current in the CDM clamps, and typically has a value of about 200-400 ohms, although it may be higher or lower than those values.

As shown in Fig. 2, CDM clamp diode 116 between nodes A and B may be implemented as grounded-gate NMOS device 202. As shown in Fig. 3A, CDM clamp diode 114 between nodes A and C may be implemented as a standard PN diode 302 with anode 304 formed by a boron implant in n-type well 306. n+ region 308 provides a contact to n-well 306, which forms the cathode of the diode. Alternatively, CDM clamp

diode 114 may be implemented as PMOS device 310 with its gate connected to the power supply voltage.

Referring back to Fig. 1, and as discussed hereinabove, ESD event 118 connects input pad 110 to ground, discharging any charge stored in the VDD and/or ground supply rails of the IC through input pad 110. Preferably, the parasitic resistance between a CDM clamp and its respective input transistor should generally be kept below 0.5 ohms. In the prior art, however, because the CDM clamps and the input transistors are not integrated, metal interconnects are used to connect the devices. These metal interconnects create parasitic resistance and inductance R^* between the CDM clamps and their input transistors, thus interfering with the proper operation of the CDM protection mechanism.

In a preferred embodiment of the present invention, because both of the CDM clamping diodes may be implemented using MOS devices, the CDM clamps may be integrated into the input transistors, as shown in Fig. 4. By integrating the CDM clamps into the same active area as the input transistors of the internal input circuit, the parasitic resistance and inductance are minimized between the ground/power-supply connections of the CDM clamps and the input transistors. Fig 4A illustrates integrated CDM clamp/input circuit 400 in schematic form. Fig. 4B illustrates a top down view of circuit 400 as implemented in a semiconductor substrate, while Fig. 4C illustrates a cross-section of circuit 400 as implemented in a semiconductor substrate. Note that input resistor 410 in Fig. 4A is not shown in Figs. 4B and 4C. Ground node 402, input node 404, output node 406 and power supply node 408 are the same in each of the Figures 4A, 4B and 4C.

In Figs. 4B and 4C, the NMOS devices are formed in p-substrate 420, and the PMOS devices are formed in n-well 422. PMOS input transistor 412 in Fig. 4A comprises p+ drain 434, polysilicon gate 432, and p+ source 430 in Figs. 4B and 4C. NMOS input transistor 414 in Fig. 4A comprises n+ drain 436, polysilicon gate 438, and n+ source 440 in Figs. 4B and 4C. CDM clamp PMOS transistor 416 in Fig. 4A comprises p+ drain 426, polysilicon gate 428, and p+ source 430 in Figs. 4B and 4C. CDM clamp NMOS transistor 418 in Fig. 4A comprises n+ drain 444, polysilicon gate 442, and n+ source 440 in Figs. 4B and 4C. Of course, each of the above devices also

comprises a gate dielectric and channel underlying the gate. Contact to p-substrate 420 is provided by p+ contact 446, and contact to n-well 422 is provided by n+ contact 424.

As can be seen in Figs. 4B and 4C, PMOS input transistor 412 and CDM clamp PMOS transistor 416 share p+ source region 430 as a single source for both devices.

5 Similarly, NMOS input transistor 414 and CDM clamp NMOS transistor 418 share n+ source region 440 as a single source for both devices. A metal interconnect layer is not needed to connect the source regions of the devices, thus avoiding the parasitic resistance and inductance created by the metal interconnect of prior art devices.

10 Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, the specific transistor implementation of the inventive circuits may be varied from the examples provided herein while still remaining within the scope of the present invention. The layout and cross-section representations of the preferred embodiments are generic, and variations of the specific implementations shown are within the scope of the present invention. As other examples, p-type and n-type semiconductor regions may be switched, or the source and drain of a MOS transistor may be switched. Devices may share a different common element other than the source. Integrated circuit materials other than those disclosed herein may be used.

15 20 As another alternative, multiple transistors or other devices such as diodes may be used for the CDM clamps or input transistors, or combinations may be used. As another alternative, there may be one clamp protecting an internal circuit, or more than two clamps protecting an internal circuit. The CDM clamps may be used in conjunction with other ESD protection devices.

25 Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently

30 existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may

0220 0230 0240 0250 0300 0310 0320 0330 0340 0350 0400 0410 0420 0430 0440 0450 0500 0510 0520 0530 0540 0550 0600 0610 0620 0630 0640 0650 0700 0710 0720 0730 0740 0750 0800 0810 0820 0830 0840 0850 0900 0910 0920 0930 0940 0950 1000 1010 1020 1030 1040 1050 1100 1110 1120 1130 1140 1150 1200 1210 1220 1230 1240 1250 1300 1310 1320 1330 1340 1350 1400 1410 1420 1430 1440 1450 1500 1510 1520 1530 1540 1550 1600 1610 1620 1630 1640 1650 1700 1710 1720 1730 1740 1750 1800 1810 1820 1830 1840 1850 1900 1910 1920 1930 1940 1950 2000 2010 2020 2030 2040 2050 2100 2110 2120 2130 2140 2150 2200 2210 2220 2230 2240 2250 2300 2310 2320 2330 2340 2350 2400 2410 2420 2430 2440 2450 2500 2510 2520 2530 2540 2550 2600 2610 2620 2630 2640 2650 2700 2710 2720 2730 2740 2750 2800 2810 2820 2830 2840 2850 2900 2910 2920 2930 2940 2950 3000 3010 3020 3030 3040 3050 3100 3110 3120 3130 3140 3150 3200 3210 3220 3230 3240 3250 3300 3310 3320 3330 3340 3350 3400 3410 3420 3430 3440 3450 3500 3510 3520 3530 3540 3550 3600 3610 3620 3630 3640 3650 3700 3710 3720 3730 3740 3750 3800 3810 3820 3830 3840 3850 3900 3910 3920 3930 3940 3950 4000 4010 4020 4030 4040 4050 4100 4110 4120 4130 4140 4150 4200 4210 4220 4230 4240 4250 4300 4310 4320 4330 4340 4350 4400 4410 4420 4430 4440 4450 4500 4510 4520 4530 4540 4550 4600 4610 4620 4630 4640 4650 4700 4710 4720 4730 4740 4750 4800 4810 4820 4830 4840 4850 4900 4910 4920 4930 4940 4950 5000 5010 5020 5030 5040 5050 5100 5110 5120 5130 5140 5150 5200 5210 5220 5230 5240 5250 5300 5310 5320 5330 5340 5350 5400 5410 5420 5430 5440 5450 5500 5510 5520 5530 5540 5550 5600 5610 5620 5630 5640 5650 5700 5710 5720 5730 5740 5750 5800 5810 5820 5830 5840 5850 5900 5910 5920 5930 5940 5950 6000 6010 6020 6030 6040 6050 6100 6110 6120 6130 6140 6150 6200 6210 6220 6230 6240 6250 6300 6310 6320 6330 6340 6350 6400 6410 6420 6430 6440 6450 6500 6510 6520 6530 6540 6550 6600 6610 6620 6630 6640 6650 6700 6710 6720 6730 6740 6750 6800 6810 6820 6830 6840 6850 6900 6910 6920 6930 6940 6950 7000 7010 7020 7030 7040 7050 7100 7110 7120 7130 7140 7150 7200 7210 7220 7230 7240 7250 7300 7310 7320 7330 7340 7350 7400 7410 7420 7430 7440 7450 7500 7510 7520 7530 7540 7550 7600 7610 7620 7630 7640 7650 7700 7710 7720 7730 7740 7750 7800 7810 7820 7830 7840 7850 7900 7910 7920 7930 7940 7950 8000 8010 8020 8030 8040 8050 8100 8110 8120 8130 8140 8150 8200 8210 8220 8230 8240 8250 8300 8310 8320 8330 8340 8350 8400 8410 8420 8430 8440 8450 8500 8510 8520 8530 8540 8550 8600 8610 8620 8630 8640 8650 8700 8710 8720 8730 8740 8750 8800 8810 8820 8830 8840 8850 8900 8910 8920 8930 8940 8950 9000 9010 9020 9030 9040 9050 9100 9110 9120 9130 9140 9150 9200 9210 9220 9230 9240 9250 9300 9310 9320 9330 9340 9350 9400 9410 9420 9430 9440 9450 9500 9510 9520 9530 9540 9550 9600 9610 9620 9630 9640 9650 9700 9710 9720 9730 9740 9750 9800 9810 9820 9830 9840 9850 9900 9910 9920 9930 9940 9950 10000 10010 10020 10030 10040 10050 10100 10110 10120 10130 10140 10150 10200 10210 10220 10230 10240 10250 10300 10310 10320 10330 10340 10350 10400 10410 10420 10430 10440 10450 10500 10510 10520 10530 10540 10550 10600 10610 10620 10630 10640 10650 10700 10710 10720 10730 10740 10750 10800 10810 10820 10830 10840 10850 10900 10910 10920 10930 10940 10950 11000 11010 11020 11030 11040 11050 11100 11110 11120 11130 11140 11150 11200 11210 11220 11230 11240 11250 11300 11310 11320 11330 11340 11350 11400 11410 11420 11430 11440 11450 11500 11510 11520 11530 11540 11550 11600 11610 11620 11630 11640 11650 11700 11710 11720 11730 11740 11750 11800 11810 11820 11830 11840 11850 11900 11910 11920 11930 11940 11950 12000 12010 12020 12030 12040 12050 12100 12110 12120 12130 12140 12150 12200 12210 12220 12230 12240 12250 12300 12310 12320 12330 12340 12350 12400 12410 12420 12430 12440 12450 12500 12510 12520 12530 12540 12550 12600 12610 12620 12630 12640 12650 12700 12710 12720 12730 12740 12750 12800 12810 12820 12830 12840 12850 12900 12910 12920 12930 12940 12950 13000 13010 13020 13030 13040 13050 13100 13110 13120 13130 13140 13150 13200 132